Amendments to the Specification:

Please replace paragraph [0003] with the following amended paragraph:

[0003] U.S. Patent Application No. 09/684,034, filed May 30, 2000, now US Patent 6,920,811, and entitled "Slack Fetch to Improve Performance of a Simultaneous and Redundantly Threaded Processor." ~~(1662-23801).~~

Please replace paragraph [0004] with the following amended paragraph:

[0004] U.S. Patent Application No. 09/837,995, filed April 19, 2001, and entitled "Simultaneously and Redundantly Threaded Processor Store Instruction Comparator." ~~(1662-36900).~~

Please replace paragraph [0005] with the following amended paragraph:

[0005] U.S. Patent Application No. 09/839,621, now U.S. Pat. No. 6,598122, filed April 19, 2001, and entitled "Active Load Address Buffer." ~~(1662-37100).~~

Please replace paragraph [0006] with the following amended paragraph:

[0006] U.S. Patent Application No. 09/838,078, filed April 19, 2001, and entitled "Simultaneous and Redundantly Threaded Processor Branch Outcome Queue." ~~(1662-37200).~~

Please replace paragraph [0007] with the following amended paragraph:

[0007] U.S. Patent Application No. 09/838,069, filed April 19, 2001, now US Patent 6,792,525, and entitled "Input Replicator for Interrupts in a Simultaneous and Redundantly Threaded Processor." ~~(1662-37300).~~

Please replace paragraph [0008] with the following amended paragraph:

[0008] U.S. Patent Application No. 09/839,626, filed April 19, 2001, and entitled "Simultaneously and Redundantly Threaded Processor Uncached Load Address Comparator and Data Value Replication Circuit." ~~(1662-37400),~~

Please replace paragraph [0009] with the following amended paragraph:

[0009] U.S. Patent Application No. 09/839,624, filed April 19, 2001, and entitled "Load Value Queue Input Replication in a Simultaneous and Redundantly Threaded Processor." ~~(1662-37500),~~

Please replace paragraph [0046] with the following amended paragraph:

[0046] As shown, fetch unit 102 includes branch prediction logic 103 and a "slack" counter 104. Slack counter 104 is used to create a delay of a desired number of instructions between the threads that include the same instruction set. The introduction of slack permits the leading thread T0 to resolve all or most branch misspeculations and cache misses so that the corresponding instructions in the trailing thread T1 will not experience the same latency problems. The branch prediction logic ~~104~~ 103 permits the fetch unit 102 to speculate ahead on branch instructions as noted above. In order to keep the pipeline full (which is desirable for efficient operation), the branch predictor logic 103 speculates the outcome of a branch instruction before the branch instruction is actually executed. Branch predictor 103 generally bases its speculation on previous instructions. Any suitable speculation algorithm can be used in branch predictor 103.

Please replace paragraph [0052] with the following amended paragraph:

[0052] The architecture and components described herein are typical of microprocessors, and particularly pipelined, multithreaded processors. Numerous modifications can be made from that shown in Figure 4. For example, the locations of the RUU 130 and registers 122, 126 can be reversed if desired. For additional information, the following references, all of which are incorporated herein by reference, may be consulted for additional information if needed: U.S. Patent Application Serial No. 08/775,553, now U.S. Pat. No. 6,073,159, filed December 31, 1996, and "Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreaded Processor," by D. Tullsen, S. Eggers, J. Emer, H. Levy, J. Lo and R. Stamm, Proceedings of the 23rd Annual International Symposium on Computer Architecture, Philadelphia, PA, May 1996.